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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicants:	Tonia G. Morris, et al.	§	Art Unit:	2612
Serial No.:	09/106,994	§		
		§	Examiner:	Jason T. Whipkey
Filed:	June 29, 1998	§		
Title:	Imager Having Multiple Storage Locations for Each Pixel Sensor	§	Docket No.	ITL.0061US (P5989)

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

2/27/04 WKG

APPEAL BRIEF

Dear Sir:

Applicant hereby appeals from the Final Rejection dated September 11, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation, the assignee of the present application by virtue of the assignment recorded at Reel/Frame 9296/0068.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

Date of Deposit February 4, 2004
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Janice Munoz

III. STATUS OF THE CLAIMS

Claims 1, 3-6, 8-10 and 18-28 have been finally rejected and are the subject of this appeal.

IV. STATUS OF AMENDMENTS

There are no unentered amendments.

V. SUMMARY OF THE INVENTION

Referring to Fig. 3, an embodiment 50 of a digital imager in accordance with the invention includes an imaging semiconductor chip 54 which has a light sensing, imaging surface 51. The surface 51 is located in a focal plane onto which images to be captured are focused and includes an array 60 (see Fig. 4) of pixel sensing units 68, each of which senses an intensity of light that strikes a portion, or pixel, of the surface 51. The surface 51 is covered by an electrically programmable color filter 52 (a color filter available from ColorLink, Inc., of Boulder, Colorado, for example) which is electrically configured by the chip 54 to allow primary color components (primary color components from the set of red, green and blue primary colors, as examples) from the image to individually strike the surface 51 in succession and be detected by the pixel sensing units 68, as described below. Specification, pp. 3-4.

For this to occur, in some embodiments, the filter 52 (as described below) is configured by the chip 54 to successively cycle through three primary color modes. In each mode, the filter 52 allows a different one of the primary color components to pass through the filter 52 and strike the surface 51. As described below, each mode has a

duration that is sufficient to permit each pixel sensing unit 68 to sense the corresponding color component of the associated pixel, and after sensing the color component, each pixel sensing unit 68 locally stores a color value that is indicative of the sensed primary color component. As described below, because the color values are stored locally in the array 60, the array 60, in some embodiments, is only scanned after all primary color components are captured. Specification, p. 4.

After the color filter 52 cycles through all three modes, the array 60 is scanned to retrieve the stored color values (for all three color components). Referring to Fig. 4, each scanning of the array 60 may include successively scanning the rows of the array 60, one at a time. For example, row 63 and column 61 decoders may begin the scan by electrically selecting a group of the pixel sensing units 68 and one of the primary colors. Once selected, the pixel sensing unit 68 transfers the stored value (that corresponds to the selected color) to signal conditioning circuitry 62. The circuitry 62 may, for example, filter noise from the values before transferring the values to an output interface 64. The output interface 64 may include buffers for temporarily storing the color values and circuitry to interface the imager 50 to external circuitry (other components of a digital camera, for example). The chip 54 might also include, for example, a control unit 66 which has circuitry such as state machines and timers to control the scanning and data flow through the chip 54. The control unit 66 is coupled to selection lines 69 for selecting the stored color values in the array 60, and the control unit 66 also interacts with the color filter 52 to control the modes of the filter 52. Specification, p. 4.

The advantages of storing the color values locally in the array 60 may include one or more of the following: The primary color components of a video image may be captured before the array is scanned; true color pixel values may be retrieved from the array; and the values may be formatted into digital words on the imager. Specification, pp. 4-5.

Referring to Fig. 5, in some embodiments, the color values for each pixel sensing unit 68 may be represented by analog voltages that are stored in analog storage units 70 (units 70a, 70b and 70c, as examples). Each storage unit 70 stores a different color value. For example, if the pixel sensing unit 68 stores values for the primary colors of red, green and blue, the storage unit 70a may store the red color value, the storage unit 70b may store the green color value, and the storage unit 70c may store the blue color value. The storage units 70 may include, for example, capacitors. Specification, p. 5.

Each pixel sensing unit 68 may include a photosensitive element 72, such as a photosensitive diode, that provides an output signal (a current, for example) that indicates the intensity of light that is sensed for the pixel. Because just one element 72 may be used to detect all three primary color components, the pixel sensing unit 68 may include multiplexing circuitry (described below) to route the signal from a sampling node 91 (an output terminal of the photosensitive element 72) to the appropriate storage unit 70 based on the mode of the color filter 52 (i.e., based on which primary color component is being sensed by the array 60). Specification, p. 5.

The multiplexing circuitry includes switches to route the sensed color values to the appropriate storage unit 70. In this manner, in some embodiments (where the primary

color components of red, green and blue are being captured, for example), when the color filter 52 is allowing the red color component to pass through, a switch 73a (which is controlled by a signal called SAMPR) closes to route the output signal from the sampling node 91 to the storage unit 70a. Similarly, when the color filter 52 is allowing the green color component to pass through, a switch 73b (controlled by a signal called SAMPG) closes to route the output signal from the node 91 to the storage unit 70b. Lastly, when the color filter 52 is allowing the blue color component to pass through, a switch 73c (controlled by a signal called SAMPB) closes to route the signal from the node 91 to the storage unit 70c. When one of the switches 70a, 70b or 70c is closed, the other two switches are open. Therefore, the output signal from the photosensitive element 72 is routed to only one of the storage units 70 based on the primary color component being sensed by the array 60. Specification, pp. 5-6.

The decoders 61 and 63 (see Fig. 4) select a particular color value that is stored by the pixel sensing unit 68. In this manner, the decoders 61 and 63 activate an appropriate select signal (described below) to select both the pixel sensing unit 68 and one of the primary colors. When this occurs, the multiplexing circuitry of the pixel sensing unit 68 transfers an indication of the selected color value from the corresponding storage unit 70 to an analog-to-digital converter (ADC) 74. The ADC 74 might be, for example, a serial ADC and may be shared by more than one pixel sensing unit 68. For example, in some embodiments, the ADC 74 may be a multi-channel bit serial (MCBS) ADC as described in David X.D. Yang, Boyd Fowler & Abbas el Gamal, A Nyquist Rate Pixel Level ADC for CMOS Image Sensors, The Custom Integrated Circuit Conference,

May 1998, p. 237-40. In some embodiments, the ADC 74 converts the indication (an analog value, for example) from the storage unit 70 into digital bits that are serially communicated to the signal conditioning circuitry 62 (see Fig. 4) via a bit line 76. Specification, p. 6.

The multiplexing circuitry of the pixel sensing unit 68 also routes the indications from the storage units 70 to the ADC 74. For example, the multiplexing circuitry may include switches 75 (switches 75a, 75b and 75c, as examples). When the decoders 61 and 63 assert (drive high, for example) a select signal (called WLR) to initiate retrieval of the red color value, the switch 75a closes to couple the storage unit 70a to the ADC 74. Similarly, when the decoders 61 and 63 assert a signal (called WLG) to initiate retrieval of the green color value, the switch 75b closes to couple the storage unit 70b to the ADC 74. Lastly, when the decoders 61 and 63 assert a select signal (called WLB) to initiate retrieval of the blue color value from the unit 70c, a switch 75c closes to couple the storage unit 70c to the ADC 74. Specification, p. 6.

Referring to Figs. 7, 8, 9, 10, 11 and 12, as an example, to capture a multi-color image, the control unit 66 might first assert (drive high, for example) the SAMPR signal (at time T_0) to close the switch 73a and deassert (drive low, for example) the SAMPG and SAMPB signals. The control unit 66 keeps the SAMPR signal asserted for an integration interval (called T_{I1}) from time T_o to time T_1 during which the signal (a current signal, for example) from the node 91 is integrated by the storage unit 70a to form the stored red color value. Next, the control unit 66 deasserts the SAMPR signal at time T_1 and asserts the SAMPG signal during another integration interval (called T_{I2}) from time

T_1 to time T_2 to store the green color value in the storage element 70b in a similar manner. The control unit 66 then deasserts the SAMPG signal and asserts the SAMPB signal during another integration interval (called T_{I3}) from time T_2 to time T_3 to store the blue color value in the storage unit 70c. After all three integration intervals expire, the decoders 61 and 63 may then assert, as examples, the WLR signal (from time T_4 to time T_5), the WLG signal (from time T_5 to time T_6) and the WLB signal (from time T_6 to time T_7) to selectively couple the associated storage units 70 to the bit line 76. Specification, pp. 6-7.

Referring to Fig. 13, in some embodiments of the pixel sensing unit 68, the photosensitive element 72 includes a photosensitive diode 90 that is exposed at the surface 51 (see Fig. 3) to sense light. The cathode of the diode 90 is coupled to ground, and the anode of the diode 90 is coupled to the sampling node 91. An n-channel, metal-oxide-semiconductor field-effect-transistor 92 has its drain-source path coupled between the sampling node 91 and a positive voltage supply level (called V_{CC}). The gate of the transistor 92 is driven by a reset signal (called RESET) which is briefly asserted (driven high, for example) by the control unit 66 near the beginning of each integration interval T_{I1}, T_{I2} and T_{I3}. In this manner, referring to Fig. 6, the control unit 66 pulses high the RESET signal at the beginning of each integration interval to cause the transistor 92 to conduct and pull the voltage level of the sampling node 91 near the V_{CC} positive voltage supply level. As a result, this brief pulse 93 causes a predetermined initialization value to be stored in the storage unit 70. Specification, p. 7.

In some embodiments, the storage unit 70 might include a capacitor that is formed from an n-channel, metal-oxide-semiconductor field-effect-transistor 82. Each switch 73 (switches 73a, 73b and 73c, as examples) might include an n-channel, metal-oxide-semiconductor field-effect-transistor 80 that has its drain-source path coupled between the associated storage unit 70 and the sampling node 91. The drain of the transistor 80 forms a storage node 79 for, as an example, storing a voltage indicative of the light intensity of a specific color value. The gate of the transistor 80 is driven by the associated SAMPR, SAMPG or SAMPB signal. Specification, pp. 7-8.

Alternatively, the switch 73 may include an n-channel, metal-oxide-semiconductor field-effect-transistor that is configured as a source follower. In this manner, the source of the transistor is coupled to the storage node 79, the gate of the transistor is coupled to the sampling node 91, and the drain of the transistor receives a voltage (in place of the SAMPR signal) that turns the transistor either on or off. Specification, p. 8.

Each switch 75 might include an n-channel, metal-oxide-semiconductor field-effect-transistor 84 that has its drain-source path coupled between the V_{CC} positive voltage supply level and the bit line 76. The gate of the transistor 84 is coupled to the storage node 79. As a result of this arrangement, when the initialization value is stored in the associated storage unit 70, the storage node 79 has a positive voltage which places the transistor 84 in a linear conduction mode. As a result of this arrangement, during the integration interval, the voltage of the sampling node 79 is indicated by the source of the transistor 84. Specification, p. 8.

The switch 75 may also include an n-channel, metal-oxide-semiconductor field-effect-transistor 86 which has its drain-source path coupled in series between the source of the transistor 84 and the bit line 76. The gate of the transistor 86 is driven by the associated WLR, WLG or WLB signal which causes the transistor 86 to either conduct or not conduct. Specification, p. 8.

In other embodiments, the pixel sensing unit may include digital storage units. For example, referring to Fig. 14, a pixel sensing unit 100 includes digital storage units 102 that may, for example, replace the analog storage units 70 of the pixel sensing unit 68. In this manner, each digital storage unit 102 stores a digital value that represents a color value for the pixel. In the pixel sensing unit 100, the sampling node 91 is coupled to an input terminal of a sample and hold (SH) circuit 78. When the control unit 66 asserts (drives high, for example) a signal (called SAMPLE), the SH circuit 78 integrates and temporarily stores the signal provided by the sampling node 91. When the control unit 66 deasserts (drives low, for example) the SAMPLE signal, the SH circuit 78 transfers the resultant integrated signal to an ADC 103 (a serial ADC, for example). In some embodiments, the S/H circuit 78 may include a switch and a storage unit that are arranged in similar manner as the switch 73 and storage unit 70. The SAMPLE signal is used in place of the SAMPR, SAMPG and SAMPB signals and may be represented, in some embodiments, as a result of a logical ORing of these signals. Specification, pp. 8-9.

The digital output signal that is furnished by the ADC 103 is routed to one of the digital storage units 102. To accomplish this, each switch 101 (switches 101a, 101b and 101c, as examples) is coupled to the output terminal of the ADC 103 and to a different

one of the digital storage units 102. As an example, for the case where the red, green and blue primary color components are being sensed by the array 60, at the end of the integration interval for the red primary color, the control unit 66 asserts a signal (called SWR1) to close the switch 101a to couple the ADC 103 to the digital storage unit 102a. After a predetermined interval of time elapses (eight clock cycles, for example), the control unit 66 deasserts the SWR1 signal to decouple the ADC 103 from the storage unit 102a. The other switches 101b and 101c are coupled in a similar manner and are exclusively activated by either the SWG1 or SWB1 signals in a similar manner after the expiration of the green and blue color integration intervals, respectively. Specification, p. 9.

In some embodiments, for purposes of retrieving a color value from the pixel sensing unit 100 and furnishing that value to the bit line 76, the decoders 61 and 63 assert one of three select signals: an SWR2 signal (to select the storage unit 102a), an SWG2 signal (to select the storage unit 102b) and an SWB2 signal (to select storage unit 102c). The SWR2, SWG2 and SWB2 signals activate different switches 104, each of which is coupled between its associated digital storage unit 102 and the bit line 76. Specification, p. 9.

In other embodiments, the pixel sensing unit may have fewer storage units than the number of primary colors being sensed. For example, referring to Fig. 15, in some embodiments, a pixel sensing unit 108 may be used in place of the units 68 or 100. The pixel sensing unit 108 is identical to the pixel sensing unit 100 except that the unit 108 does not include one of the digital storage units 102, such as the digital storage unit 102c,

for example. Unlike the arrangement of the unit 100, one of the switches 101 (the switch 101c activated by the SWB1 signal, for example) is coupled between the output terminal of the ADC 103 and the bit line 76. Specification, pp. 9-10.

Due to this arrangement, an indication of the blue primary color component, for example, may be transferred directly from the ADC 103 to the bit line 76 without requiring temporary storage. As a result, the pixel sensing unit 108 may consume less semiconductor die area. Specification, p. 10.

In some embodiments, a pixel sensing unit may be arranged similarly to the pixel sensing unit 108 except that this pixel sensing unit does not include the switch 101c. In this manner, the decoders 61 and 63 retrieve the stored color value from either the storage unit 102a or 102b before the ADC 103 processes the third color value (a blue color value, for example). In this manner, the control unit 66 may activate the appropriate switch 101a or 101b to store the third color value in the storage unit 102a or 102b from which the stored color value has already been retrieved. Specification, p. 10.

Referring to Fig. 16, in some embodiments, the imager 50 may be part of a digital camera 110. Besides the imager 50, the camera 110 may include optics 160 which form an image on the imaging surface 51 (see Fig. 4) of the imager 50. In some embodiments, the camera 110 includes a scaling unit 166 that may, for example, scale up or down the resolution of a transmitted image before communicating it to a bus 120 (a serial bus, for example) that is used for communication with, for example, a computer. The camera 110 may also include a compression unit 168 and a bus interface unit 170 to interact with the

bus 120. To coordinate activities of these units, the camera 110 may include a microprocessor 162. Specification, p. 10.

VI. ISSUES

A. Can claims 1, 3-5 and 26 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

B. Can claims 6, 8-10 and 27 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 6?

C. Can claims 18-21 and 28 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 18?

D. Can claims 22-25 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 22?

E. Can claims 25-28 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for any of these claims?

VII. GROUPING OF THE CLAIMS

Claims 1 and 3-5 can be grouped together; claims 6 and 8-10 can be grouped together; claims 18-21 can be grouped together; claims 22-24 can be grouped together; and claims 25-28 can be grouped together. With this grouping, all claims of a particular group stand or fall together. Furthermore, regardless of the grouping that is set forth by the Examiner's rejections, the claims of each group set forth in this section stand alone with respect to the claims of the other groups that are set forth in this section. In other words, any claim of a particular group that is set forth in this section does not stand or fall together with any claim of any other group that is set forth in this section.

VIII. ARGUMENT

All claims should be allowed over the cited references for the reasons set forth below.

A. Can claims 1, 3-5 and 26 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 1?

The imager of independent claim 1 includes an array of pixel sensors. Each pixel sensor indicates at least two different primary color components of an image. The imager includes, for each pixel sensor, at least two storage locations that are located in the array to store the indications from the pixel sensor; and each storage location is designated for a different one of the primary color components of the image. The image sensor includes, for each pixel sensor, circuitry to, during a first integration interval, couple the pixel sensor to one of the associated storage locations to store one of the indications from the sensor and during a second integration interval, couple the pixel sensor to another one of the storage locations to store another one of the indications from the sensor.

The Examiner rejects independent claim 1 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,754,229 (herein called "Elabd") in view of U.S. Patent No. 4,845,540 (herein called "Baker"). Both Baker and Elabd are generally directed to imaging devices.

More specifically, Elabd generally discloses various embodiments of an image sensor and associated circuitry. For example, in one embodiment, Elabd discloses an arrangement that includes an image register 452 and a storage register 454. *See, for*

example, Figure 1 of Elabd. Elabd discloses that the image register 452, "receives light from a colored image, integrates the charge packets produced by a succession of n color exposures, and delivers them, one exposure at a time, to light-shielded memory sites or storage registers 454." Elabd, 4:7-13. Elabd neither teaches nor suggests that light is integrated in the storage registers 454, but rather, Elabd teaches that the image register 452 receives light from the colored image and integrates the charge packets produced by these exposures.

In Figure 3, Elabd discloses another embodiment that includes an image register 486 and a storage register 490. Elabd states that the charge packets from successive color exposures may be stored in the storage register 490 sequentially. *See, for example*, Elabd, 5:14-25. Similar to the other disclosed embodiments, Elabd neither teaches nor suggests that any integration is performed via the storage register 490. In other words, Elabd neither teaches nor suggests that during an integration interval, any storage location in the storage register 490 is coupled to a pixel sensor. Rather, Elabd teaches that *after* integration, the integrated values are transferred from the image register 486 to the storage register 490.

Thus, Elabd fails to teach or suggest all claim limitations. Namely, Elabd fails to teach or suggest an image sensor that during integration intervals couples pixel sensors to different storage locations, where the storage locations are associated with different primary color components. Instead, Elabd teaches an arrangement that during a particular color exposure, the locations of the image register 486 in which integration occurs are all associated with the same primary color component.

Because Elabd fails to teach or suggest all claim limitations, the Examiner relies on the modification of Elabd to derive the claimed invention. More particularly, the Examiner relies on Baker to allegedly provide the suggestion or motivation for the modification of Elabd so that Elabd's image sensor integrates the exposures directly in the storage register 490. Baker generally discloses an imaging device that includes multiple storage locations for each sensing pixel in which integration occurs. For example, Figure 2 of Baker shows two capacitors 2a and 2b for a photodiode 1. The photodiode 1 produces a current in response to light during an exposure, and this current is integrated by one of the capacitors 2a and 2b for purposes of storing a voltage on the capacitor 2a, 2b to indicate an integrated value.

Baker's invention relates to increasing a throughput of its imaging device as compared to pixel sensors of the prior art in which readout of the value stored in the integrating capacitor could not be obtained until integration was complete. Due to Baker's use of two capacitors 2a and 2b, the photodiode 1 may integrate into one of the capacitors 2a and 2b while a previously-integrated value is read out from the other capacitor 2a, 2b. Thus, throughput of the imaging device improved. However, Baker does not teach or suggest integrating different color components into the capacitors 2a and 2b nor does Baker teach or suggest associating the capacitors 2a, 2b with different primary color components.

The Examiner's rejection of independent claim 1 is based on the modification of Elabd in view of Baker. In other words, the Examiner's rejection of claim 1 is based on the premise that one skilled in the art, without knowledge of the claimed invention, would

have modified Elabd in view of Baker so that Elabd's image register 486 is bypassed, and color values are integrated directly into the storage register 490, a register that associates different locations with different colors. However, the Examiner fails to support this position and instead bases the modification of Elabd on pure hindsight gleaned from the current application.

"Obviousness cannot be predicated on what is unknown." *In re Spormann*, 363 F.2d 444, 448, 150 USPQ 449, 452 (CCPA 1966). Thus, to establish a *prima facie* case of obviousness, the Examiner must show, with specific citations to the prior art, where the prior art contains the alleged suggestion or motivation for the modification of Elabd to derive the claimed invention. *In re Rijckaert*, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); and M.P.E.P. § 2143. However, as set forth below, the Examiner fails to show the existence of such a suggestion or motivation, as the Examiner's conclusion of obviousness assumes knowledge of the claimed invention.

In an attempt to show where the prior art allegedly contains the suggestion or motivation for the modification of Elabd, the Examiner, in the Final Office Action, refers to lines 46-52 in column 9 of Baker. This cited passage, however, refers to the advantage of having two capacitors for integration, in that while light is being integrated via one capacitor, a stored integrated value may be read out from the other capacitor. The Examiner contends that this language would have lead one skilled in the art to modify Elabd so that light is integrated directly into the storage registers 490, thereby bypassing the integration of storage elements by the image register 486. However, the cited language does not support this conclusion.

Rather, the cited language may, at most, arguably motivate one skilled in the art to include multiple integrating capacitors in Elabd's image register for each pixel. Thus, by including multiple integration capacitors in the image register, this would reduce any delay between integrations by the image register, as taught by Baker, in that one capacitor of the image register may be integrating while another capacitor may be furnishing a previously-integrated value. However, without the hindsight gleaned from the claimed invention, one skilled in the art would not have been motivated to modify Elabd so that Elabd's integration bypasses the image register altogether and instead relies on the storage elements of the storage register as the integrating elements. The Examiner merely concludes that such a suggestion or motivation for this modification exists, without showing where the prior art contains the alleged suggestion or motivation.

Thus, a *prima facie* case of obviousness has not been established for independent claim 1. Claims 3-5 and 26 are patentable for at least the reason that these claims depend from an allowable claim. Therefore, the § 103(a) rejections of claims 1, 3-5 and 26 are in error and should be reversed.

B. Can claims 6, 8-10 and 27 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 6?

The camera of independent claim 6 includes an array of pixel sensors. Each pixel sensor indicates at least two color components of an image. The camera includes a programmable color filter to substantially cover the array and a controller to control the color filter to cause the pixel sensors to indicate the color components one at a time. For

each pixel sensor, the camera includes at least two storage locations that are located in the array to store the indications from the pixel sensor, and each storage location is designated for a different one of the primary color components of the image. The camera also includes, for each pixel sensor, circuitry to, during a first integration interval, couple the pixel sensor to one of the associated storage locations to store one of the indications from the sensor and, during a second integration interval, couple the pixel sensor to another one of the storage locations to store another one of the indications from the sensor.

The Examiner rejects independent claim 6 under 35 U.S.C. § 103(a) over Elabd in view of Baker. More specifically, the Examiner's rejection of independent claim 6 is based on the modification of Elabd's image sensor so that the image register 486 of Elabd is bypassed and integration occurs directly in the storage register 490. The Examiner attempts to provide the alleged suggestion or motivation for this modification by citing language from Baker. However, Baker merely discloses two integrating capacitors for each pixel sensor. Baker does not associate either of these storage elements with a particular color or with different colors, but rather, Baker's system is directed to increasing the throughput through the image sensor so that the value stored by one storage capacitor may be read while integration is being performed in another storage capacitor. Baker does not, however, associate either one of these storage capacitors with a particular color component.

Even assuming, *arguendo*, that a suggestion or motivation exists for the combination of Baker and Elabd, the Examiner fails to show where the prior art contains

the alleged suggestion or motivation to modify Elabd so that integration bypasses the image register of Elabd's imaging device and integrates values directly in the storage register. More specifically, combining Baker and Elabd arguably yields, at best, multiple integrating capacitors in the image register, not the replacement of Elabd's image register 486 with circuitry to directly integrate color component values in the storage register 490. Thus, the Examiner's rejection is based on the hindsight gleaned from the application, and the Examiner fails to show where the prior art contains the alleged suggestion or motivation for this modification to derive the claimed invention.

Claims 8-10 and 27 are patentable for at least the reason that these claims depend from an allowable claim. Thus, the § 103(a) rejections of claims 6, 8-10 and 27 are improper and should be reversed.

C. Can claims 18-21 and 28 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 18?

The method of independent claim 18 includes providing a pixel sensor and providing at least two storage locations that are associated with the pixel sensor. Each storage location is designated for a different primary color component of an image. The method includes during a first integration interval, coupling the pixel sensor to one of the associated storage locations to storage an indication from the pixel sensor; and during a second integration interval, coupling the pixel sensor to another one of the storage locations to store another indication from the pixel sensor.

The Examiner rejects independent claim 18 under 35 U.S.C. § 103(a) in view of the combination of Elabd and Baker. However, the method of independent claim 18 recites that during a first integration interval, the pixel sensor is coupled to a storage location that is designated for one primary color component and during a second integration interval, the pixel sensor is coupled to a storage location that is designated for a different primary color component.

Combining Baker and Elabd would, at most, arguably produce a system in which two storage locations that are designated *for the same primary color component* to the pixel sensor during integration. (emphasis added). The Examiner, based on the knowledge gleaned from the claimed invention, modifies Elabd so that integration bypasses Elabd's image register and occurs directly in Elabd's storage register. However, the Examiner's position is untenable, as the Examiner fails to show the alleged suggestion or motivation in the prior art for this modification of Elabd.

Claims 19-21 and 28 are patentable for at least the reason that these claims depend from allowable claim. Thus, the § 103(a) rejections of claims 18-21 and 28 are in error and should be reversed.

D. Can claims 22-25 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for independent claim 22?

The imager of independent claim 22 includes an array of pixel sensors and at least two integration devices for each pixel sensor. Each integration device is designated to provide a value for a different primary color.

The Examiner rejects independent claim 22 under 35 U.S.C. § 103(a) in view of the combination of Elabd and Baker. However, this combination of references fails to teach or suggest at least two integration devices for each pixel sensor where each integration device is designated to provide a value for a different primary color. More specifically, although Elabd shows a storage register 490 that receives integrated values *after* integration, Elabd integrates these color components in an image register 486 before passing the integrated values to the storage registers. Although Baker discloses multiple storage locations per pixel, Baker, at most, arguably provides a suggestion or motivation to modify Elabd so that Elabd's image register, not its storage register, contains multiple storage locations per pixel. However, neither reference, alone or in combination, teaches or suggests at least two integration devices for each pixel sensor, where each integration device is designated to provide a value for a different primary color.

Claims 23-25 are patentable for at least the reason that these claims depend from an allowable claim. Thus, the § 103(a) rejections of claims 22-25 are improper and should be reversed.

E. Can claims 25-28 be rendered obvious when the Examiner has failed to establish a *prima facie* case of obviousness for any of these claims?

Claim 25 depends from independent claim 22 and recites that the integration devices of claim 22 include at least three integration devices for each pixel sensor. Claims 26, 27 and 28 depend from claims 1, 6 and 18, respectively, and each recite that the storage locations include at least three storage locations for each pixel sensor.

Claims 25-28 are patentable for at least the reason that these claims depend from allowable, independent claims, for the reasons set forth above in the discussion of Issues A-D above. These claims are also patentable based on at least the additional, independent reason that the Examiner fails to establish a *prima facie* case of obviousness for the additional limitations that are presented by these claims.

More specifically, the Examiner rejects claims 25-28 under 35 U.S.C. § 103(a) in view of the combination of Elabd and Baker. However, Baker only discloses *two* storage capacitors per pixel cell. *See, for example,* Figure 2 of Baker. In Figure 7, Baker depicts three capacitors per pixel cell, however, only two of these capacitors are used for storage locations. The third capacitor for each pixel cell is coupled in parallel with one of the other two storage capacitors. *See, for example,* Baker, 10:43-65. Thus, none of the arrangements that are disclosed in Baker teaches or suggests at least three integration devices per pixel, for the case for the integration devices are each designated to provide a value for a different primary color. Furthermore, neither of the arrangements that are disclosed in Baker teaches or suggests at least three storage locations for each pixel sensor, where each storage location is designated for a different color component.

Thus, Baker fails to teach or suggest the additional limitations that are presented by claims 25-28. Furthermore, Elabd fails to teach or suggest these claim limitations, as Elabd does not teach or suggest multiple integrating storage locations per pixel cell. Therefore, for at least the reason that the combination of Elabd and Baker fails to teach or suggest the additional limitations that are presented by dependent claims 25-28, a *prima facie* case of obviousness has not been established for any of these claims.

Therefore, the § 103(a) rejections of claims 25-28 are improper and should be reversed.

IX. CONCLUSION

Applicant requests that each of the final rejections be reversed and that the claims subject to this appeal be allowed to issue.

Respectfully submitted,

Date: February 4, 2004

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APPENDIX OF CLAIMS

The claims on appeal are:

1. An imager comprising:

an array of pixel sensors, each pixel sensor to indicate at least two different primary color components of an image;

for each pixel sensor, at least two storage locations located in the array to store the indications from the pixel sensor and each storage location being designated for a different one of the primary color components of the image; and

for each pixel sensor, circuitry to, during a first integration interval, couple the pixel sensor to one of the associated storage locations to store one of the indications from the sensor and, during a second integration interval, couple the pixel sensor to another one of the storage locations to store another one of the indications from the sensor.

3. The imager of claim 1, wherein the circuitry includes an analog-to-digital converter to convert the indications from the pixel sensor into a digital format.

4. The imager of claim 1, wherein the indications comprise analog signals.

5. The imager of claim 1, wherein the indications comprise digital signals.

6. A camera comprising:

an array of pixel sensors, each pixel sensor to indicate at least two color components of an image;

a programmable color filter substantially covering the array;

a controller to control the color filter to cause the pixel sensors to indicate the color components one at a time;

for each pixel sensor, at least two storage locations located in the array to store the indications from the pixel sensor and each storage location being designated for a different one of the primary color components of the image; and

for each pixel sensor, circuitry to, during a first integration interval, couple the pixel sensor to one of the associated storage locations to store one of the indications from the sensor and, during a second integration interval, couple the pixel sensor to another one of the storage locations to store another one of the indications from the sensor.

8. The camera of claim 6, wherein the circuitry includes an analog-to-digital converter to convert the indications from the pixel sensor into a digital format.

9. The camera of claim 6, wherein the indications comprise analog signals.

10. The camera of claim 6, wherein the indications comprise digital signals.

18. A method comprising:

providing a pixel sensor;

providing at least two storage locations associated with the pixel sensor and each storage location being designated for a different primary color component of an image;

during a first integration interval, coupling the pixel sensor to one of the associated storage locations to store an indication from the pixel sensor; and

during a second integration interval, coupling the pixel sensor to another one of the storage locations to store another indication from the pixel sensor.

19. The method of claim 18, wherein

one of the indications from the pixel sensor indicates a first primary color component; and

another one of the indications from the pixel sensor indicates another primary color component different from the first primary color component.

20. The method of claim 18, further comprising:

converting the indications from the pixel sensor into a digital representation; and

storing the digital representations in the storage locations in response to the coupling.

21. The method of claim 18, further comprising:

forming a pixel sensor array that includes the pixel sensor.

22. An imager comprising:

an array of pixel sensors; and

at least two integration devices for each pixel sensor, each integration device being designated to provide a value for a different primary color.

23. The imager of claim 22, wherein each of said at least two storage locations are associated with different color components.

24. The imager of claim 22, wherein each of said at least two storage locations are associated with different primary color components.

25. The imager of claim 22, wherein said at least two integration devices comprise at least three integration devices for each pixel sensor.

26. The imager of claim 1, wherein said at least two storage locations comprise at least three storage locations for each pixel sensor.

27. The camera of claim 6, wherein said at least two storage locations comprise at least three storage locations for each pixel sensor.

28. The method of claim 18, wherein said at least two storage locations comprise at least three storage locations for each pixel sensor.

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TRANSMITTAL OF APPEAL BRIEF (Large Entity)

Docket No. ITL.0061US

In Re Application Of: **Tonia G. Morris et al.**

Serial No.	Filing Date	Examiner	Group Art Unit
09/106,994	06/29/98	Jason T. Whipkey	2612

Invention: **Imager Having Multiple Storage Locations For Each Pixel Sensor**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

The fee for filing this Appeal Brief is: **$330.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

Dated: **February 4, 2004**

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I certify that this document and fee is being deposited on **February 4, 2004** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Janice Munoz

Signature of Person Mailing Correspondence

Janice Munoz

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